FIG 1

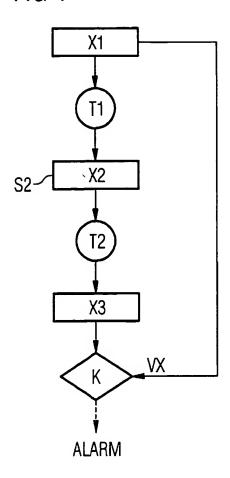


FIG 2

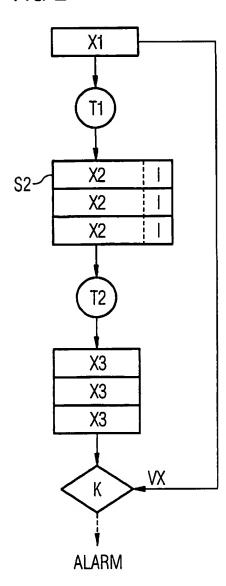


FIG 3

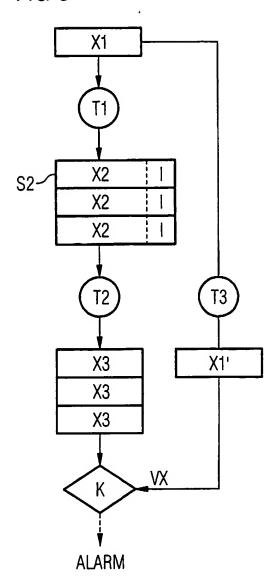


FIG 4

MEM

DEC 3

R1 COMP

ALARM

FIG 5

MEM

DEC

R2

R1

CPU

ALARM